

High-Mobility, Heterostructure Light-Emitting Transistors and Complementary Inverters

Mujeeb Ullah,[†] Kristen Tandy,[†] Jun Li,[‡] Zugui Shi,[‡] Paul L. Burn,[†] Paul Meredith,[†] and Ebinazar B. Namdas^{*,†}

[†]Centre for Organic Photonics & Electronics, School of Mathematics and Physics, School of Chemistry and Molecular Biosciences, The University of Queensland, Brisbane, QLD 4072, Australia

[‡]Institute of Materials Research and Engineering, Agency for Science, Technology and Research, Singapore 117602

Supporting Information

ABSTRACT: Light-emitting field effect transistors (LEFETs) are optoelectronic devices that can simultaneously execute light emission and the standard logic functions of a transistor in a single device architecture. In this article, we show that ambipolar LEFETs can be made in a bilayer structure using Super Yellow, a light-emitting polymer layer, and a high-mobility diketopyrrolo-pyrrole-based copolymer as an ambipolar charge-transporting layer. The LEFETs were fabricated in the bottom gate architecture with top-contact, air-stable, symmetric Au–Au electrodes. The devices show light emission in both electron and hole accumulation modes with an external quantum efficiency (EQE) of 0.1% at a brightness of 650 cd/m² in electron accumulation mode. We have also



demonstrated a light-emitting inverter by combining two LEFETs into the inverter architecture. The light-emitting inverter generates both electrical and optical signals with an electrical gain of 112.

KEYWORDS: ambipolar, organic semiconductor, light-emitting transistor, inverter

ight-emitting field effect transistors (LEFETs) are an emerging class of multifunctional optoelectronic devices. LEFETs combine the electroluminescence properties of organic light-emitting diodes (OLEDs) with the switching properties of transistors in a single architecture.¹⁻²⁷ The dual functionality of LEFETs has the potential for new applications such as simplified pixels for flat panel displays and optoelectronic devices in communications. However, before LEFETs can reach their potential in optoelectronic applications it will be necessary to achieve substantially improved charge carrier mobilities and balanced transport in the active layers, develop less reactive electrodes, and use more highly luminescent materials.^{1-3,15-18} Over the past decade important steps toward addressing these issues have been made. Particular effort has been directed toward the device architectures with single-layer,^{1-10,12-14} bilayer,^{15,16,19} heterostructure (multilayer),^{17,18} and split gates,¹¹ all being explored as a means to improve performance. Heterostructure LEFETs are comprised of a luminescent layer deposited on a high-mobility transport layer^{15,16} or sandwiched between hole and electron charge transport layers.^{17,18} However, the majority of heterostructure LEFETs operate mainly in the p-channel regime, in which the holes accumulate across the transistor channel in the charge mobility layer, with injection directly into the emissive layer by a low-work-function metal electrode. It is critical for the integration of LEFETs into circuits for logic operations to have devices that work in both pand n-mode.

In this report we demonstrate solution-processed heterostructure ambipolar LEFETs operating in both p- and n-mode with the highest hole mobility of 0.4 cm² V⁻¹ s⁻¹ and electron mobility of 0.15 cm² V⁻¹ s⁻¹. We demonstrate that bilayer LEFETs fabricated using air-stable, symmetric Au–Au electrodes give an emission brightness of 650 cd/m² with an external quantum efficiency (EQE) of 0.1% in electron accumulation (nchannel) mode and a brightness of 4 cd/m² with an EQE of 0.001% in hole accumulation mode (p-channel). Furthermore, by changing one of the electrodes to calcium we have created devices with a brightness of 850 cd/m² and an EQE of 0.09% in n-channel mode and 900 cd/m² at an EQE of 0.04% in pchannel mode. By connecting two identical ambipolar LEFETs, we demonstrate a light-emitting inverter. The light-emitting inverter exhibits both electrical and optical characteristics.

Figures 1a and b show the molecular structures of the charge transport material, diketopyrrolo-pyrrole based copolymer (DPP-DTT)²⁸ and emissive material Super Yellow (SY) poly(1,4-phenylenevinylene) copolymer, which were used in this study. The LEFETs were fabricated using 400 nm of SiNx as the dielectric on highly n-doped silicon substrates with an additional poly(methyl methacrylate) (PMMA) dielectric passivation layer. The DPP-DTT was then spin-coated onto the PMMA followed by the emissive layer of SY. The devices

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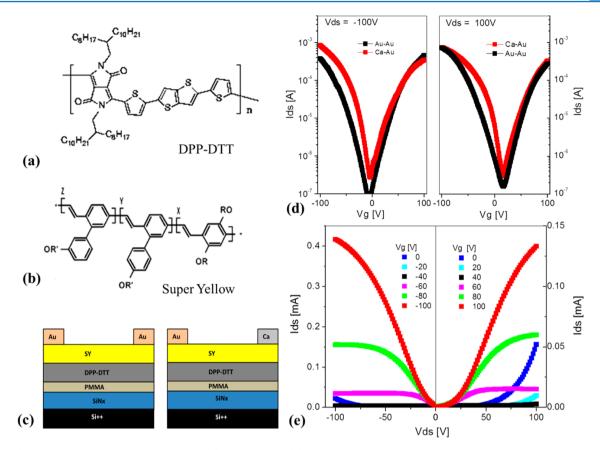


Figure 1. (a) Molecular structures of DPP-DTT and (b) Super Yellow; (c) device schematics of the heterostructure LEFETs with symmetric Au–Au electrodes and asymmetric Ca–Au electrodes; (d) electrical transfer characteristics of the typical LEFETs; (e) output characteristics of an LEFET with Au–Au electrodes. (Output characteristics for an LEFET with Ca–Au electrodes are given in Figure S1 in the Supporting Information.)

Table 1. Comparison of LEFET Performance with Symmetric (Au-Au) and Asymmetric Electrodes (Ca-Au)^a

emissive layer	Super Yellow	
electrodes	Au-Au	Ca–Au
$\mu_{ m hole} \; [m cm^2 \; V^{-1} \; s^{-1}]$	0.40 ± 0.1	0.5 ± 0.1
$\mu_{ m electron} \; [m cm^2 \; V^{-1} \; s^{-1}]$	0.15 ± 0.05	0.2 ± 0.1
ON/OFF ratio	>10 ³	>10 ³
max EQE [%]	0.1 ± 0.05	0.25 ± 0.1
maximum brightness [cd m ⁻²] (electron accumulation mode, $V_g > 0$)	650 ± 50	850 ± 50
EQE at maximum brightness [%] (electron accumulation mode, $V_g > 0$)	0.1 ± 0.05	0.09 ± 0.02
maximum brightness [cd m^{-2}] (hole accumulation mode, Vg < 0)	4 ± 1	900 ± 50
EQE at maximum brightness [%] (hole accumulation mode, $V_g < 0$)	0.001 ± 0.08	0.04 ± 0.01
width of emission zone	$8 \pm 1 \ \mu m$	$6 \pm 1 \ \mu m$
ambient shelf life at $V_{\rm g}$ = -100 V (when $I_{\rm ds}$ becomes half of its initial value)	>48 h $(I_{ds} \text{ did not decrease in 48 h})$	<1 min
ambient shelf life at $V_{g} = 100 \text{ V}$ (when I_{ds} becomes half of its initial value)	30 h	<1 min

^aThe \pm represent the standard deviation of the mean as derived from the averages of multiple devices.

were completed by deposition of the source and drain electrodes, which were either symmetric (Au-Au) or asymmetric (Ca-Au). The completed device geometries of the heterostructure LEFETs are shown in Figure 1c. All the devices were fabricated and tested inside nitrogen-filled gloveboxes (<5 ppm O₂ and H₂O). Further details of the fabrication procedures are presented in the Experimental Section and the Supporting Information.

Figure 1d shows the electrical transfer characteristics of LEFETs with symmetric (Au–Au) and asymmetric (Ca–Au) electrodes. The output characteristics of the Au–Au LEFETs for n-channel mode [gate voltage (V_g) > 0] and p-channel mode ($V_g < 0$) are shown in Figure 1e. The corresponding plots for the Ca–Au LEFETs are shown in Figure S1. For both device architectures in n-mode, at low gate voltages (0 to 20 V) the drain current increased rapidly with increasing source–

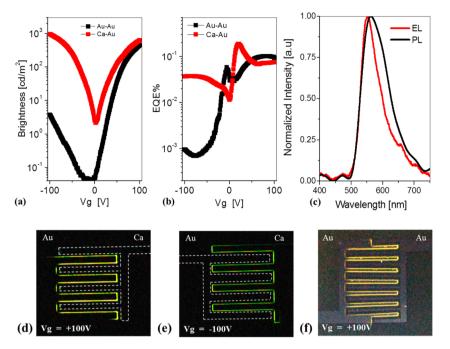


Figure 2. (a) Optical transfer characteristics of the LEFETs ($V_{ds} = -100$ V); (b) external quantum efficiency as a function of gate voltage; (c) electroluminescence (EL) and photoluminescence (PL) emission spectra of the LEFETs; (d) microscope image of an asymmetric Ca–Au LEFET in n-channel mode ($V_g = 100$ V) and (e) p-channel mode ($V_g = -100$ V). (f) Microscope image of a symmetric Au–Au LEFET in n-channel mode ($V_g = 100$ V).

drain voltage. In this regime, both electrons and holes are injected from the source and drain electrodes into the SY and DPP-DTT layers in a similar manner to a light-emitting diode, which we will call "diode-like" operation throughout the discussion of the results. At higher positive gate voltages of +40 to +100 V the transistor operated fully in n-channel accumulation mode with distinct linear and saturation regions for low (0–20 V) and high (20–100 V) source–drain voltages, respectively. Similarly, in p-type mode, at low gate voltages (–0 to – 20 V) the device operated diode-like with the transport of both electrons and holes; then at gate voltages of -40 to -100 V, the transistor operated fully in p-channel accumulation mode with the normal linear and saturation regions for low and high values of source–drain voltages.

The charge carrier mobilities were calculated from the saturation regime of the transfer characteristics of the LEFETs. For the Ca–Au devices the hole and electron mobilities were $0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively (see Table 1). Interestingly, the LEFETs with symmetric Au–Au contacts had similar hole and electron mobilities in the saturated regime (Table 1). Although the active channel is composed of two polymers, the origin of the high electron and hole mobilities is mainly due to charge transport occurring in the DPP-DTT layers.²⁸ While DPP-DTT has been reported to have a hole mobilities observed in the LEFETs are due to the top SY layer having a higher contact resistance for charge injection into the DPP-DTT layer.¹⁷ A switching on/off ratio of $\geq 10^3$ was observed in all the LEFET devices (see Table 1).

The optical transfer characteristics of the LEFETs are shown in Figure 2a. A brightness of 650 cd/m^2 with a quantum efficiency of 0.1% was observed in n-channel mode for the device with the symmetric Au–Au electrodes, while relatively modest light emission was observed (4 cd/m^2) in p-channel mode. For the asymmetric Ca–Au electrode case, a brightness of 900 cd/m² was achieved with an EQE of 0.09% in n-mode, while 950 cd/m² and an EQE of 4×10^{-2} % was measured in pchannel mode. The reason for the significantly better emission performance in hole accumulation mode for the Ca–Au electrode combination is due to the fact that the injection barrier for electrons into the emissive layer is less for the Ca than the Au electrode. The photoluminescence spectra and electroluminescence spectra of LEFET devices are given in Figure 2c, and their similarity shows that both EL and PL occur from the same emissive states.

The details of the operating mechanism along with energy levels are given in the Supporting Information (see Figure S3). In n-channel mode, $V_g > 0$, electrons are injected from the source electrode, Ca or Au, into the DPP-DTT (~-3.5 eV) layer via the SY layer. In this LEFET operation mode, electrons are accumulated and are the majority carrier in the LEFET channel at $V_g > 40$ V. These electrons move across the LEFET channel and pass into the light-emitting polymer in order to reach the drain electrode under source–drain bias. At the same time holes are injected from the Au electrode into the light-emitting layer, which results in exciton formation and light emission in the vicinity of the hole-injecting Au electrode, as shown in Figure 2d for the asymmetric electrode and Figure 2f for the symmetric electrode devices.

In p-channel mode, $V_g < 0$, holes are injected from the Au electrode into the DPP-DTT, again via the SY layer. In this case holes are the major carrier species in the channel, and for the asymmetric electrode combination, electrons are injected from the Ca electrode into the light-emitting layer, leading to formation and recombination of excitons near the Ca electrode (see Figure 2e). For the symmetric Au–Au contacts, the barrier height for electron injection from Au into SY is much higher and hence results in weak light emission in the p-channel mode. However, an important point with regard to the use of the symmetric Au–Au contacts is that the LEFETs show more

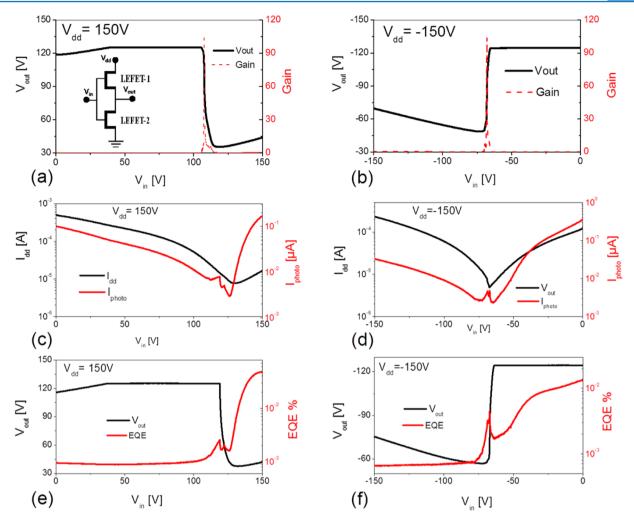


Figure 3. (a, b) Complementary inverter characteristics and voltage gains of symmetric LEFETs for the electron and hole channels. Inset of (a) shows an inverter circuit schematic using two identical LEFETs. (c, d) Complementary inverter characteristics showing drain current and photocurrent during the inverter operation. (e, f) Inverter output voltage and external quantum efficiency (EQE) of inverter.

stable characteristics (for both p- and n-mode), whereas the devices fabricated with the Ca–Au electrodes stopped working if exposed (<1 min) to oxygen and moisture. This is mainly due to the very high reactivity of Ca to moisture and oxygen. The drain current and photocurrent obtained from LEFETs fabricated with Au–Au electrodes as a function of storage time in air can be seen in Figure S4. Even after 50 h in air, the drain current and photocurrent of the LEFETs do not decrease significantly. We note that the DPP-DTT polymer is stable in the ambient environment, with reports that OFET charge carrier mobility and on/off ratio do not change over a period of a year.²⁸

In a final aspect of the study, complementary MOS-like voltage inverters were fabricated using two identical LEFETs with symmetric Au–Au electrodes on the same substrate. Figure 3a and b show the output voltage and gain of the inverter. An inverter gain of 110 was observed in the first quadrant and 112 in the third quadrant, which is excellent for an inverter based on LEFETs with symmetric Au–Au electrodes. The optical characteristics of the inverter are given in Figures 3c and d, which show that the light emission follows the patterns of the output voltages in both the third and first quadrants. The EQEs (calculated from inverter characteristics given in Figures 3c and d) show an opposite trend to the

inverter output voltage in the first quadrant and the same trend as the inverter output voltage in the third quadrant, as shown in Figures 3e and f.

Insight into how the light-emitting inverter works can be obtained by looking at the voltage transfer, drain current, and light emission characteristics presented in Figure 3 and Figures S5-S7. For simplicity, the operation of the light-emitting inverter can be divided into three main regions: $V_{in} = 0$ to -60V (region A); $V_{in} = -60$ to -75 V (region B); and $V_{in} = -75$ to -15 V (region C). For LEFET-1 when V_{in} is scanned from 0 V to -60 V (region A) and the output voltage is held at -125 V(source-drain voltage difference = -25 V), the device moves from diode-like performance to fully p-mode. In this process LEFET-1 emits light, although weakly, as is the case of the single LEFET discussed earlier. LEFET-2 has a source-drain voltage of -125 V, meaning that it still emits light from a diodelike mode. Region B ($V_{in} = -60$ to -75 V) involves the nearly vertical segment of the transfer characteristics, where both of the transistors operate in the saturation regime and the same current flows through both LEFETs. Due to low gate and source-drain voltages of both LEFETs, the total current flowing in the device is at the minimum value, and weak light emission was detected from both LEFETs (see Figure 3d). In region C ($V_{in} = -75$ to -150 V) LEFET-1 is ON and operates

in saturation p-mode with weak light emission when V_{d-s} is around -90 V. While LEFET-2 also operates in a hole accumulation mode, no light is observed, which we attribute to the lower source-drain voltage with respect to LEFET-1. We have noted a shift in the inverter transition in Figure 3a in electron accumulation mode; this is mainly due to imbalanced mobilites (for electrons and holes) and the bias stress in the channel.

In the case where $V_{\rm in}$ is positive the inverter still has an excellent gain of 110. Under low positive $V_{\rm in}$ (<100 V) both LEFETs function in the diode-like mode, while at higher $V_{\rm in}$ (>100 V) they operate in n-channel mode. Table S2 shows a detailed comparison (in five regions) of a conventional CMOS inverter, an organic semiconductor transistor-based inverter and LEFET inverter. At low $V_{\rm in}$ both LEFETs emit light while in diode-like operation. In addition, when $V_{\rm in}$ is >100 V, similar levels of light emission are observed and the EQE is higher. This is in contrast to when $V_{\rm in}$ is negative and arises from the fact that the electron density in the device is driven by $V_{\rm in}$ and not limited to direct injection from the Au electrode into the SY. The improved output of the inverter operating with $V_{\rm in}$ being positive is consistent with the LEFET results discussed earlier.

In summary, we have demonstrated high electron and hole mobilities and brightnesses in an LEFET using solutionprocessed semiconducting polymer heterostructures. For an LEFET that contained air-stable Au source and drain electrodes, light emission was visible with brightnesses exceeding 650 cd/m² and an EQE of 0.1% at the highest brightness. Light emission intensity and position were found to strongly depend on the gate bias, which is the first time this has been seen for a heterostructure LEFET. The operating voltage can be reduced by further implementing a number of approaches including reducing the channel length and increasing the gate capacitance and using materials with high mobility. We have also demonstrated a light-emitting inverter by combining the LEFET into an inverter architecture. We are able generate two output signals that have transfer characteristics with a record gain of 112.

EXPERIMENTAL SECTION

The heterostructure LEFETs were fabricated using heavily ndoped Si wafers with a 400 nm SiNx dielectric layer grown by the low-pressure physical vapor deposition technique, which were purchased from Silicon Quest, International, Inc. The substrates were precisely diced to give dimensions of 15 mm \times 15 mm before being cleaned in a Class 1000 clean room by ultrasonication in acetone for 15 min, followed by 15 min in 2propanol. The cleaned substrates were dried using pressurized nitrogen and were transferred into a nitrogen glovebox $(O_2 and$ H₂O level < 0.1 ppm). Fabrication and testing were performed in gloveboxes. An additional 120 nm thick dielectric passivation layer of PMMA (120 000 g mol⁻¹) was spin-coated onto the SiNx from a solution with a concentration of 30 mg mL⁻¹ in *n*propyl acetate (\geq 99.5%) at 2500 rpm for 30 s. After the PMMA deposition the substrates were annealed on a hot plate at 150 °C for 30 min. The film thicknesses were measured using a Dektak 150 profilometer. A DPP-DTT polymer layer,²⁸ synthesized at IMRE, Singapore ($M_n = 125\ 000\ g/mol;\ M_w =$ 349 000 g/mol), was then deposited on top of the PMMA layer by spin-coating a 4 mg mL⁻¹ solution in a mixture of chloroform (99.9%, anhydrous) with 7% chlorobenzene (by volume) (\geq 99%, anhydrous). The solution was heated at 80 °C

to dissolve the DPP-DTT polymer fully and then spin-coated hot at 1000 rpm for 60 s. The substrates were then annealed at 150 °C for 30 min. Finally an emissive layer of Super Yellow [(PDY-132) was purchased from Merck and used without further purification] was deposited on top of the DPP-DTT layer by spin-coating from a 7 mg mL⁻¹ solution in toluene (>99.9%, anhydrous) at 2500 rpm for 30 s, then at 3000 rpm for 10 s. The substrates were then again baked on the hot plate at 150 °C for 30 min.

For the devices with symmetric top Au source–drain electrodes, both electrodes were deposited in a single evaporation (see Figure 1). In the case of the asymmetric top electrodes, the interdigitated source and drain contacts were formed by vacuum evaporation of Au and Ca using two complementary shadow masks with the same dimensions as the substrates (see Figure 1c). In this case the Au electrode was deposited before the Ca. The transistor channel width was 16 mm and the length was 100 μ m. A total of at least five devices were used to calculate averages. Errors were calculated using the standard deviation of the results.

Electrical and optical characterization of the LEFETs was performed using an Agilent B1500A semiconductor device analyzer and an SA-6 Semi-Auto probe station and a photomultiplier tube (pmt). The pmt was calibrated and positioned over the devices as described previously.^{17,19} The source-drain current in the LEFET channel and photocurrent in the pmt were recorded to determine the device parameters. The emission brightnesses of the LEFETs were calculated from the photocurrent in the pmt by comparison with a SY OLED of known brightness and light emission area and then corrected according to the measured emission area of the LEFETs. A digital camera connected with an optical microscope was used to capture the emission images and estimate the light-emitting area as reported previously.^{17,19} The EQE was calculated (assuming Lambertian emission) using the brightness, sourcedrain current, and emission spectrum of the device.^{17,19} The charge carrier mobilities and threshold voltage were calculated from the transfer characteristics in the saturation regime, using the equation

$$I_{\rm ds} = \frac{W C_{\rm i}}{2 L} \mu (V_{\rm g} - V_{\rm th})^2$$

where $I_{\rm ds}$ is the source–drain current, *W* is the channel width, *L* is the channel length, μ is the field-effect mobility, $C_{\rm i}$ is the geometric capacitance of the dielectric, $V_{\rm th}$ is the threshold voltage, and $V_{\rm g}$ is the gate voltage. The total capacitance of the SiNx/PMMA dielectric layer was calculated by adding the capacitance of the two dielectric layers in series.

ASSOCIATED CONTENT

Supporting Information

Materials and processing information is given in Table S1. Output characteristics for LEFETs are given in Figures S1, S2, and S7. Working mechanism of devices is shown in Figure S3. Figure S4 shows the shelf life of an LEFET with Au–Au electrodes. Inverter characteristics and schematics of operation are depicted in Figure S5. A comparison of CMOS, ambipolar, and LEFET inverters is given in Table S2. This material is available free of charge via the Internet at http://pubs.acs.org.

AUTHOR INFORMATION

Corresponding Author

Notes

The authors declare no competing financial interest.

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